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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/982,829	10/22/2001	Yong-Suk Go	8733.080.10	8486

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EXAMINER

KOVALICK, VINCENT E

ART UNIT

PAPER NUMBER

2673

DATE MAILED: 04/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/982,829

Applicant(s)

GO, YONG-SUK

Examiner

Vincent E Kovalick

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 14 January 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-15 and 25-33 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-3, 6-8, 14, 25-27, 29 and 30 is/are rejected.
- 7) ☒ Claim(s) 4, 5, 9-13, 15, 28 and 31-33 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                             | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____  |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)         | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Response to Applicant's Remarks*

1. This Office Action is in response to Applicant's Remarks, dated February 14, 2003, in response to PTO Office Action dated November 14, 2002.
2. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).
3. As to applicant's remarks relative to the use of "Official Notice"; in said PTO Office Action of November 14, 2002, no mention was made of Official Notice.
4. Applicant's understanding of the criteria necessary to establish a *prima facie* case as stated in said Remarks, is correct.
5. Regarding applicant's remarks relative to claim 1 and 25, Applicant argues that Watney (USP 5,930,398) does not teach "at least two bit lines, each bit line transmitting a bit signal having a voltage level". Watney teaches a video image, applied via a input bus to a means for compressing and encoding the data (col. 6, lines 25-39), it being well known and in common practice in the art that the data being transmitted over the bus is represented by voltages on the bus lines. It being understood that a data bus would included at least two bit lines and associated

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data control lines and that the signals communicated over the bus lines are represented by various voltage levels. Shau (USP 6,404,670) teaches voltage control means for controlling the bit-line to have a bit line voltage higher, lower and within a medium voltage range between a first and second voltage (col. 28, lines 45-47 and lines 60-63). It being understood that the means to provide a voltage control means could be extended to providing two (or "n") voltage control means. Kobayashi et al. (USP 4,859,871) teaches a D/A converter, the integrator and the analog adder constitute an essential part of a voltage level setting circuit (col. 13, lines 27-30).

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watney (USP 5,930,398) taken with Shau (USP 404,670) in view of Kobayashi et al (USP 4,859,871). Relative to claims 1 and 25, Watney **teaches** a method and apparatus for determining a quantizing factor for multi-generation data compression/decompression processes (col. 3, lines 22-67; col. 4, lines 1-67 and col. 5, lines 1-16). Watney further **teaches** a bus compressing apparatus comprising at least two bit lines, each bit line transmitting a bit signal having a voltage level (col. 6, lines 25-39 and Fig. 2). It being understood that data transmission means include data (bit) lines and that the data is represented by voltage levels.

Watney **does not teach** at least two voltage control means (voltage converters) connected to the corresponding bit lines, wherein each voltage control means changes the voltage level of the bit

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line at a different ratio from the other voltage control means; or adder means for adding voltage levels outputted from the two voltage control means to generate an analog signal.

Shau **teaches** devices having first level bit lines connected along different layout directions (col. 4, lines 1-67; col. 5, lines 1-11). Shau further **teaches** at least two voltage control means (voltage converters) connected to the corresponding bit lines, wherein each voltage control means changes the voltage level of the bit line at a different ratio from the other voltage control means (col. 28, line 43-47).

Watney taken with Shau **does not teach** adder means for adding voltage levels outputted from the two voltage control means to generate an analog signal.

Kobayashi et al. **teaches** a voltage level setting circuit (col. 2, lines 61-68 and col. 3, lines 1-36).

Kobayashi et al. further **teaches** adder means for adding voltage levels outputted from the two voltage control means to generate an analog signal (col. 13, lines 27-30).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the device as taught by Watney the features as taught by Shau in view of Kobayashi et al. in order to include in the system those features necessary to transmit the bit data being input to the at least two voltage converter and in turn generate an analog signal.

Regarding claim 6, Kobayashi et al. **teaches** a bus compression apparatus wherein the adder means performs a wired sum operation (col. 13, lines 27-30). It being understood that the means for, and concept of, wired summing is in common practice in the art.

8. Claims 2-3 and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watney taken with Shau in view of Kobayashi et al. as applied to claims 1 and 25 respectively in item 7 hereinabove, and further in view of Ng et al. (USP 5,847,616).

Regarding claims 2-3 and 26-27 Watney taken with Shau in view of Kobayashi et al. **does not teach** said bus compressing apparatus wherein the two voltage control means includes a first

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voltage control means comprising a first resistor and a second voltage control means comprising a second resistor; and wherein the first resistor and the second resistor have different resistance. Ng et al. **teaches** an embedded voltage controlled oscillator with minimum sensitivity to process and supply (col. 2, lines 31-64). Ng et al. further **teaches** two voltage control means includes a first voltage control means comprising a first resistor and a second voltage control means comprising a second resistor; and wherein the first resistor and the second resistor have different resistance (col. 7, lines 29-38).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the device as taught by Watney taken with Shau in view of Kobayashi et al. the feature as taught by Ng et al. in order to provide the first and second voltage control means with circuit structure that would facilitate changing the voltage level of the bit line of a first voltage control at a different ratio from a second voltage control means.

9. Claims 7, 14 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furuhashi et al. (USP 5,850,540) taken with Smeets et al. (USP 6,218,968) in view of Taguchi (USP 5,815,080).

Relative to claims 7 and 29, Furuhashi et al. **teaches** a method and apparatus for timesharing CPU system bus in an image generation system (col. 3, lines 64-67; col. 3, lines 1-67; col. 4, lines 1-67 and col. 5, lines 1-53). Furuhashi et al. further **teaches** a bus decompressing apparatus compressing: receiving means for receiving an analog signal formed by compressing at least n-bit data, wherein n is an integer (col. 2, lines 46-54 and col. 3, lines 9-18 and 41-56). Furuhashi et al. **does not teach** quantizing means for quantizing the analog signal from the receiving means; and coding means connected to the quantizing means for coding the quantized analog signal to reconstruct the n-bit data; or a plurality of level detectors parallelly connected to the input line to output a quantized signal.

Smeets et al. **teaches** a method for encoding data (col. col. 1, lines 42-67 and col. 2, lines 1-59).

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Smeets et al. further **teaches** quantizing means for quantizing the analog signal from the receiving means; and coding means connected to the quantizing means for coding the quantized analog signal to reconstruct the n-bit data (col. 12, lines 41-44).

Furuhashi et al. taken with Smeets et al. **does not teach** a plurality of level detectors parallelly connected to the input line to output a quantized signal.

Taguchi **teaches** a communication apparatus (col. 1, lines 41-67 and col. 2, lines 1-9). Taguchi further **teaches** a plurality of level detectors parallelly connected to the input line to output a quantized signal (col. 4, lines 6-13).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the devices of Furuhashi et al. the features as taught by Smeets et al. in view of Taguchi in order to put in place the means necessary to decompress compressed data and reconstruct the signal being processed for presentation to a display device.

Regarding claim 14, it would have been obvious to a person of ordinary skill in the art at the time of the invention that the coding means transforms the quantized analog signal to n-bit digital signals in that this is well known in the art and in common practice.

10. Claims 8 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Furuhashi et al. taken with Smeets et al. in view of Taguchi as applied to claims 7 and 29 respectively in item 9 hereinabove, and further in view of Kondo (USP 6,222,398).

Relative to claims 8 and 30, Furuhashi et al. taken with Smeets et al. in view of Taguchi **does not teach** a bus decompressing apparatus wherein quantizing means includes at least ( $2 \text{ to the } n \text{ power} - 1$ ) level detectors connected in parallel between the receiving means and the coding means, each level detector being configured to detect different voltage levels of the analog signal.

Kondo **teaches** a voltage detection circuit (col. 2, lines 43-56). Kondo further **teaches** quantizing means includes at least ( $2 \text{ to the } n \text{ power} - 1$ ) level detectors connected in parallel

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between the receiving means and the coding means, each level detector being configured to detect different voltage levels of the analog signal (col. 2, lines 43-56).

It would have been obvious to a person of ordinary skill in the art at the time of the invention to incorporate in the device as taught by Furuhashi et al. taken with Smeets in view of Taguchi the feature as taught by Kondo in order to put in place the circuitry necessary to detect the various voltage levels associated with the compressed analog signal.

***Allowable Subject Matter***

11. Claims 4-5, 9-13, 15, 28, and 31-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Relative to claims 4 and 28, the prior art of record **does not teach** a bus compressing apparatus wherein the resistance value of the second resistor of the second voltage control means is  $\frac{1}{2}$  to the  $n$  power of the resistance value of the first resistor, in which  $n$  is an integer.

Regarding claim 5, the prior art of record **does not teach** a bus compressing apparatus wherein the resistance value of the second resistor of the second voltage control means is  $\frac{1}{2}$  of the resistance value of the first resistor.

Relative to claims 9 and 31, the prior art of record **does not teach** a bus decompressing apparatus wherein each one of the level detectors comprises: a transistor controlled by the analog signal from the receiving means; and output voltage control means connected to the transistor to output the quantized analog signal to the coding means in response to the analog signal.

Regarding claim 13, the prior art of record **does not teach** a bus decompressing apparatus wherein the quantizing means includes first, second and third level detectors, each level detector having a transistor with a threshold voltage, the transistor being connected between a first voltage and a second voltage, wherein the transistor of the first level detector turns on when the

analog signal is above the second voltage, the transistor of the second level detector turns on when the analog signal is above the second voltage by about 1/3 of the difference between the first and second voltages, and the transistor of the third level detector turns on when the analog signal is above the second voltage by about 2/3 of the difference between the first and second voltage.

***Conclusion***

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U. S. Patent No.	6,064,771	Migdal et al.
U. S. Patent No.	5,883,925	Sinibaldi et al.
U. S. Patent No.	4,951,139	Hamnilton et al.

13. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

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***Responses***

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vincent E Kovalick whose telephone number is 703 306-3020. The examiner can normally be reached on Monday-Thursday 7:30- 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703 305-4938. The fax phone numbers for the organization where this application or proceeding is assigned are 703 872-9314 for regular communications and 703 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 306-0377.

  
Vincent E. Kovalick  
April 17, 2003



BIPIN SHALWALA  
SUPERVISORY PATENT EXAMINER  
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